(12) UK Patent Application (19) GB (11) 2 157 085 A

(43) Application published 16 Oct 1985

(21) Application No 8508567

(22) Date of filing 2 Apr 1985

(30) Priority data

(31) 8405220 (32) 3 Apr 1984 (33) FR

(51) INT CL⁴
H05K 3/40

(52) Domestic classification
H1R AL

(56) Documents cited
None

(58) Field of search
H1R

(71) Applicant
Rogers Corporation (USA-Massachusetts),
Main Street, Rogers, Connecticut, United States of America

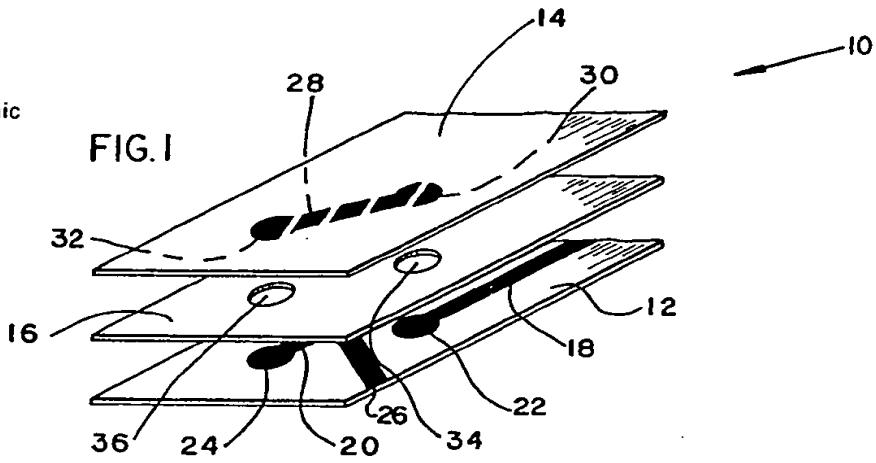
(72) Inventors
Mary T. Caton,
Frederick A. Balash,
Roger Meleard

(74) Agent and/or Address for Service
Frank B. Dehn & Co.,
Imperial House, 15-19 Kingsway, London WC2B 6UZ

(54) Multilayer flexible circuit with ultrasonically welded interlayer connections

(57) A multilayer flexible circuit (10) in which polymer thick film (PTF) circuits (18, 20, 28) are separated by an insulating polymer layer (16). The circuits are itnerconnected by ultrasonic welds, the circuit traces having enlarged connection pads (22, 24, 30, 32) in the areas of the welds.

FIG. 1



GB 2 157 085 A

2157035

FIG. 1

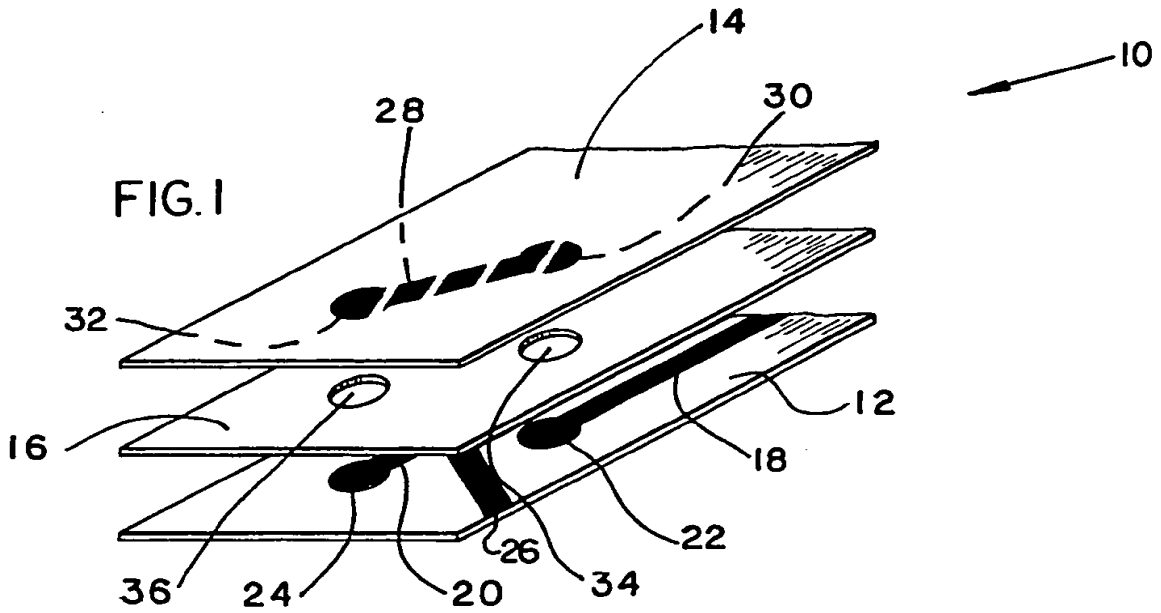


FIG.2

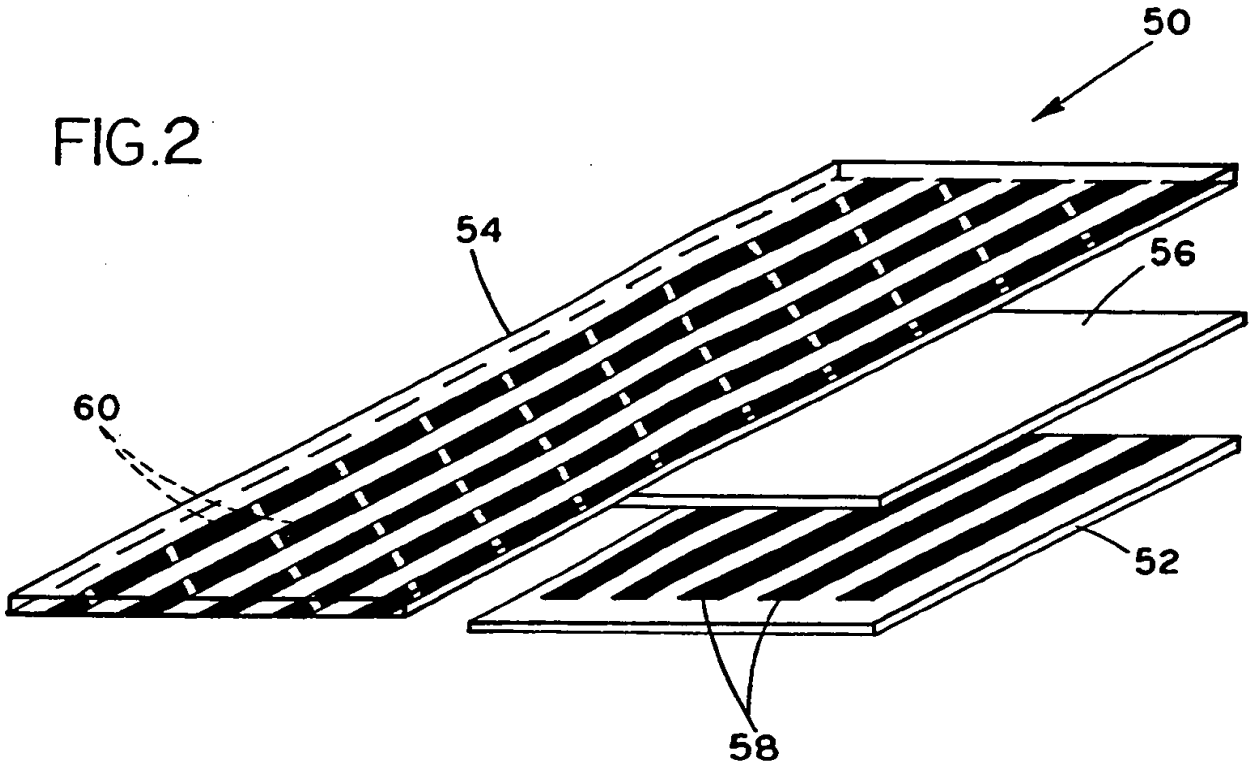
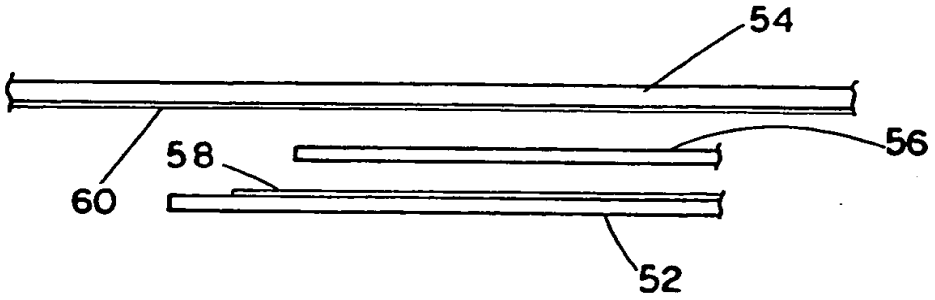


FIG.3



2157035

FIG. 4A

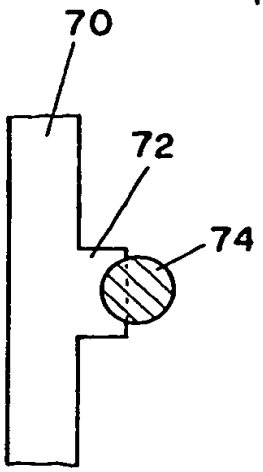


FIG. 4B

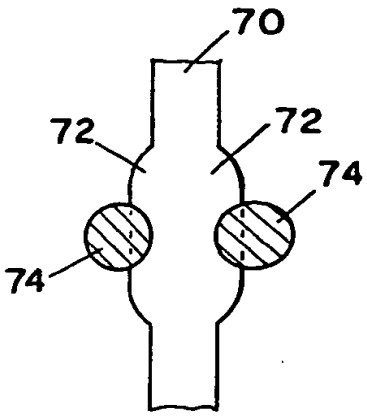


FIG. 4C

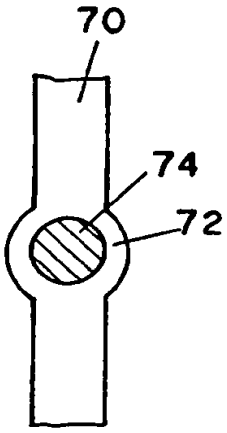


FIG. 4D

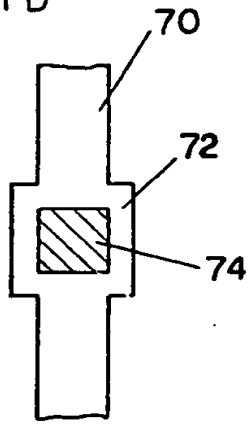


FIG. 4E

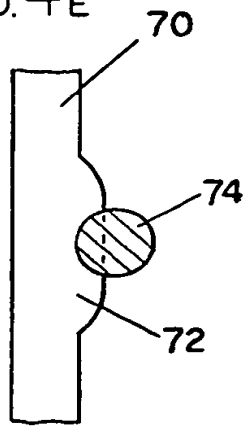


FIG. 5c

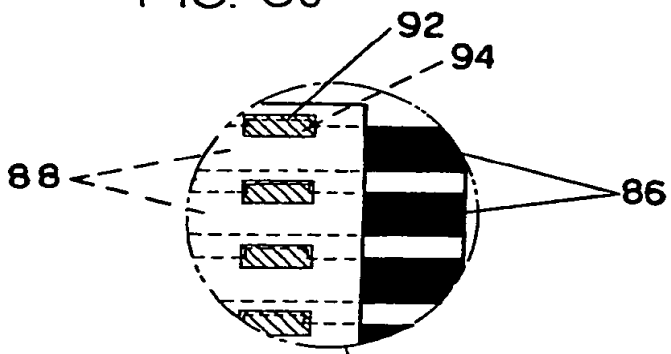


FIG. 5

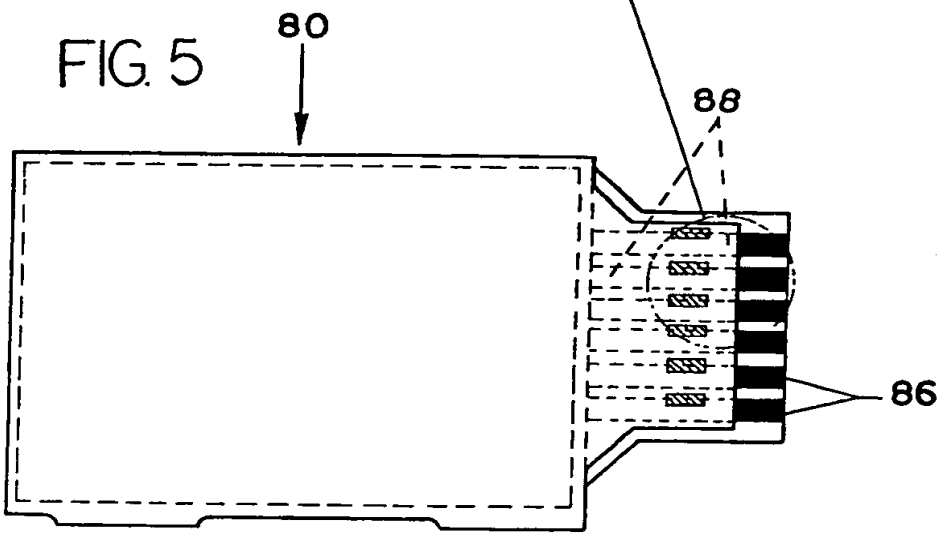


FIG. 5B

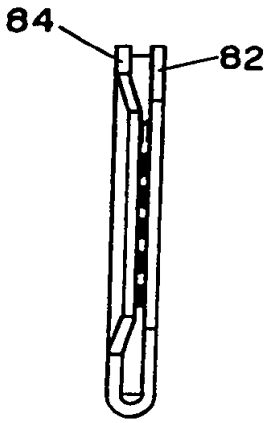
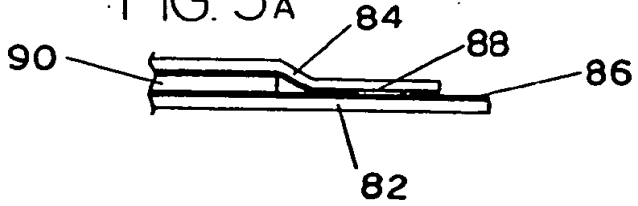


FIG. 5A



SPECIFICATION

Multilayer flexible circuit with ultrasonically welded interlayer connections

This invention relates to the field of electrical circuit connection. More particularly, this invention relates to interconnections between multilayer flexible circuits in which the circuits consist of circuit traces or circuit patterns on insulating polymer substrates.

Multilayer flexible circuits are known in which the circuits are made with polymer thick film (PTF) technology. These circuits include sheets of flexible polymer substrate material with circuit patterns thereon. The insulating substrate materials may be, for example, a polyester plastic such as Mylar (RTM) or other known plastic insulating materials; and the conductive traces may be conductive ink or paste or copper or other standard conductive trace materials for flexible circuitry and membrane keyboards. It is often desirable to interconnect two layers of flexible circuitry which face each other. Currently there are three main methods for providing such interconnection. One method is to form a conformal coating of insulating material over the appropriate traces and then use a conductive ink to close the connection between the two layers by crossing oVer the insulating material. A second method is to separate the conductive traces by a nonconductive insulating layer and make the connections by plating through holes through the insulating layer at the appropriate locations. A third method is to separate the conductive traces by a nonconductive insulating layer except in areas where connections are to be made, and connections are made by metallic crimps which pass through the two layers of conductive circuitry and hold in contact the conductive traces to be connected. These methods are plagued with reliability problems due to either migration through the conformal coating of insulating material, and/or to voids in the conductive material in the through holes, and/or poor crimp connections. Also, these methods require expensive materials and/or processing steps.

There is a recognized need for a long lasting, reliable and relatively inexpensive interconnection method and structure which has not heretofore been available in the art.

The above discussed and other problems of the prior art are eliminated or reduced by the present invention. In accordance with the present invention there is provided a multilayer circuit configuration including a first circuit layer having at least one first conductive trace thereon, a second circuit layer having at least one second conductive trace thereon, said first and second traces being in facing relationship, said first and second conductive traces each having an enlarged connection pad of predetermined configuration at opposed locations, and ultrasonic weld means interconnecting said first and second traces at said enlarged connection pads.

The termination pads are of special shape to effect reliable and permanent contact. The resulting interconnected multilayer flexible circuitry is reliable and relatively inexpensive.

It has also been determined that specific interconnect patterns contribute to improved reliability and dependability.

Referring now to the drawings, wherein like elements are numbered alike in the several Figures:

Figure 1 shows an exploded schematic view of one multilayer circuit in accordance with the present invention.

Figure 2 shows an exploded view of another multilayer circuit in accordance with the present invention.

Figure 3 shows a side elevation of the multilayer circuit of Figure 2.

Figures 4A, 4B, 4C, 4D and *4E* show specific interconnect configurations in accordance with the present invention.

Figures 5-5C show a foldover circuit with the top and bottom layers interconnected with a special interconnect pattern in accordance with the present invention. Figure 5 shows a top plan view of the foldover circuit; Figure 5A shows a partial side elevation; Figure 5B shows a front edge view (looking at the right had end of Figure 5); and Figure 5C shows an enlargement of the interconnect area.

Referring to Figure 1, an exploded view is shown of a multilayer circuit 10. Multilayer circuit 10 has a lower circuit sheet 12, an upper circuit sheet 14, and an intermediate insulating spacer sheet 16. Lower circuit sheet 12 has conductive traces 18 and 20 on the upper surface thereof which terminate in interconnection pads 22 and 24. Merely for purposes of illustration, another conductive trace 26 is shown on circuit sheet 12 between conductive traces 18 and 20. The presence of conductive trace 26 does, however, make it impossible to connect traces 18 and 20 on circuit sheet 12; so, it it is desired to interconnect traces 18 and 20, the interconnection must be made through upper circuit sheet 14.

The lower surface of circuit sheet 14 (i.e., the surface facing sheet 12) has a conductive trace 28 with termination pads 30 and 32 which are aligned, respectively, with termination pads 22 and 24 on the upper surface of circuit sheet 12. Conductive trace 28 is shown in dashed or broken line merely to indicate that it is on the bottom surface of sheet 14. Also, insulating spacer layer 16 has a pair of apertures 34 and 36 which are aligned with termination pads 22 and 30 and terminations pads 24 and 32, respectively.

To assemble the multilayer circuit of the present invention, the circuit layers 12 and 14 and the separating insulating layer 16 are brought together in the alignment shown in Figure 1, with the circuit traces facing each other and separated by insulating layer 16. With this alignment, termination pad 22 is in alignment with termination pad 30 through aperture 34, and termination pad 24 is in alignment with termination pad 32 through aperture 36. The sheets are brought together in an assembly with spacer sheet 16 sandwiched between circuit sheets 12 and 14. The assembly of the three sheets may

be adhesively bonded together at selected points if desired.

Electrical interconnection between termination pads 22 and 30 and between termination 24 and 32 is effected by ultrasonically welding the aligned termination pads to each other through the respective apertures in sheet 16. The resulting structure is a multilayer interconnected circuit with a long lasting reliable and relatively inexpensive interconnect system.

The interconnebout involvement and complications which might otherwise be present from the prior art interconnect systems such as plated through holes and conformal coatings. Furthermore, the interconnect system of the present invention lends itself particularly well to the design of interconnections which are particularly reliable. To this end, several particularly preferred termination pad and interconnection layouts are shown in Figures 4A-4E.

Figures 2 and 3 show the present invention employed to interconnect circuit layers of a type which, in the prior art, were typically connected by crimp connectors. In this embodiment, a multilayer circuit 50 has a lower circuit sheet 52, an upper circuit sheet 54 and an insulating spacer 56. Lower circuit sheet 52 has conductive traces 58 and upper circuit sheet 54 has conductive traces 60. The circuit segments to be interconnected may, for example, be tail areas of flexible circuits.

As best seen in Figure 3, insulating layer 56 stops short of the end of circuit layer 52, so that conductive traces 58 and 60 are exposed to each other at facing locations. In a typical prior art construction, costly crimp connectors would be used to connect together circuit sheets 52 and 54 in the area where traces 58 and 60 are exposed to each other, thus effecting electrical contact between the conductive traces on the two circuit sheets. In accordance with the present invention, the facing and exposed conductive traces are connected together by ultrasonic welds to deliver power or signals from one circuit sheet to the other, thus eliminating the costly crimp connectors and achieving positive and reliable interconnection.

It is to be understood that the present invention involves more than the elemental structure of ultrasonic weld interconnection. The present invention is also directed to specific interconnect configurations in the areaof the weld. When effecting the ultrasonic weld, care must be taken to ensure that the weld does not interfere with circuit functions, such as, for example, by changing circuit resistance. To this end, in accordance with the present invention the circuit traces to be interconnected are modified in shape in the area t traces to be connected (e.g., the lower and upper traces 18, 20 of Figure 1 or the lower and upper traces 58, 60 of Figure 3) will be specially and similarly shaped in the connection pad areas.

While the connection pad enlargement may take several shapes (as shown in Figures 4A-4E or other shapes), the basic parameter of the enlarged connection pad is that it does not adversely affect rsistivity or other electrical parameters of the traces being connected.

Figures 5-5C show a typical foldover circuit 80 (such as is common in a flexible circuit keyboard) with lowei layer 82 and upper layer 84 interconnected by an ultrasonic weld in accordance with the present invention. Lower cirouit sheet 82 has conductive traces 86 on its upper surface, and upper circuit sheet 84 has conductive traces 88 on its lower surface. For simplicity of illustration, these conductive traces are shown only in the end or tail area where connection is to be made, but it will understood that they continue in desired patterns on the remainder of the sheets. The upper and lower circuit sheets are separated by an insulating spacer 90 except in the area where ultrasonic weld connections are to be made (or holes can be located in the spacer at the weld position).

As best seen in Figure 5,, the circuit traces (both 86 and 88) are enlarged at 92, and are connected together at the site of the enlargement by an ultrasonic weld 94. Thus, power or a signal in traces 86 is delivered to the respective connected traces 88.

CLAIMS

1. A multilayer circuit configuration including :
a first circuit layer having at least one first conductive trace thereon,
a second circuit layer having at least one second conductive trace thereon,
said first and second traces being in facing relationship,
said first and second conductive traces each having an enlarged connection pad of predetermined configuration at opposed locations, and
ultrasonic weld means interconnecting said first and second traces at said enlarged connection pads.

2. A multilayer circuit configuration as claimed in Claim 1, wherein said connection pads are configured to meet the parameter of effecting electrical connection without impairing electrical characteristics of said traces.

3. A multilayer circuit configuration as claimed in Claim 1, wherein said connection pads are configured to effect electrical connection without impairing red in Claim 4, wherein said enlarged area is rectangular.

6. A multilayer circuit configuration as claimed in Claim 4, wherein said enlarged area is arcuate.

7. A multilayer circuit configuration as claimed in Claim 4, wherein said enlarged area is circular.

8. A multilayer circuit configuration as claimed in any one of Claims 1 to 7, including insulating spacer means between said first and second circuit layers to insulate said layers other than in said contact pad areas.

9. A multilayer circuit configuration substantially as hereinbefore described and as illustrated in the accompanying drawings.

Printed in the UK for HMSO, D8818935, 8/85, 7102.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.